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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/526,758	08/03/2005	Koichi Ooya	SONY JP 3.3-325	6906

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LERNER, DAVID, LITTENBERG,
KRUMHOLZ & MENTLIK
600 SOUTH AVENUE WEST
WESTFIELD, NJ 07090

EXAMINER	
NGUYEN, HIEU P	
ART UNIT	PAPER NUMBER
2817	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	03/14/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/526,758	OOYA ET AL.	
	Examiner	Art Unit	
	Hieu P. Nguyen	2817	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-6 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-6 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Specification

Applicant is required to update the status (pending, allowed, etc.) of all parent priority applications in the first line of the specification. The status of all citations of US filed applications in the specification should also be updated where appropriate.

The specification has not been checked to the extent necessary to determine the presence to all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

Drawings

Figures 8-12 should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g). Corrected drawings in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless --

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1 and 3 are rejected under 35 U.S.C. 102(e) as being anticipated by Behzad et al. (U.S. 6,472,940).

Regarding claim 1, Behzad discloses in Fig. 14 a variable-gain amplifier (PGA) comprising: a plurality of dual-gate FETs having first FETs (M1/M2/M3) having respective gates for being supplied with an input signal (IN) and second FETs (M51/M52/M53) having respective sources connected respectively to drains of the first FETs, the first FETs having respective sources connected in common to each other and the second FETs having respective drains connected in common to each other as shown in Fig. 14; and a plurality of voltage control means (VC1/VC2/VC3/) connected to respective gates of the second FETs for applying gate voltages separately thereto, **meeting claim 1**.

Regarding claim 3, Behzad inherently discloses the variable-gain amplifier according to claim 1 or 2, wherein the FETs for being supplied with the input signal have substantially identical electric characteristics, since they are all implemented using FETs, **meeting claim 3**.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person

having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 4 and 6 are rejected under 35 U.S.C. 103(a) as being unpatentable over Behzad.

Regarding claim 4, Behzad discloses everything claimed as applied to claim 1 (or 2) except for "wherein at least one of the FETs for being supplied with the input signal has electric characteristics different from electric characteristics of the other one or more of the FETs for being supplied with the input signal". However it would have been *prima facie* obvious to one of ordinary skill in the art at the time the invention was made to implement FETs with e.g. different sizes (W/L) depending on applications, **meeting claim 4**.

Regarding claim 6, the limitations of claim 6 (see applicant's Fig. 7) recite the "differential" version of claim 1 (see applicant's Fig. 1). However it would have been *prima facie* obvious to one of ordinary skill in the art at the time the invention was made to implement the circuit of Behzad as a differential one to handle differential input signal, since it has been held that a recitation with respect to the manner in which a clamed apparatus is intended to be employed does not differentiate the claimed apparatus from a prior art apparatus satisfying the claimed structural limitation, **meeting claim 6**.

Claims 2 is rejected under 35 U.S.C. 103(a) as being unpatentable over Behzad in view of Rowser et al. (U.S. 6,917,336).

Regarding claim 2, similar to claim 1, Behzad discloses in Fig. 14 a variable-gain amplifier comprising: a plurality of variable-gain amplifying elements having first FETs (e.g. M1/M2/M3) having respective gates for being supplied with an input signal and second FETs (e.g. M51/M52/M53) having respective source connected respectively to drains of the first FETs,

the first FETs having respective sources connected in common to each other and the second FETS having respective drains connected in common to each other; and a plurality of voltage control means (e.g. VC1/VC2/VC3) connected to respective gate of those second FETs for applying base voltages separately thereto. Behzad fails to disclose the second FETs are bipolar transistor. However, Rowser discloses in Fig. 2 an analogous circuit along with a cascode arrangement of a FET (4b) and a BJT (4a) as shown in Fig. 2. It would have been *prima facie* obvious to one of ordinary skill in the art at the time the invention was made to incorporate the teaching of Rowser into the circuit of Behzad by substituting the second FETs with bipolar transistors. The ordinary artisan would have been motivated to modify the circuit of Behzad in the manner set forth for at least the purpose of obtaining high gain as mentioned by Rower in col. 3, lines 57, **meeting claim 2**.

Claim 5 is rejected under 35 U.S.C. 103(a) as being unpatentable over Behzad in view of **Kakuta** et al. (U.S. 6,028,487).

Regarding claim 5, Behzad discloses everything claimed as applied to claim 1 except for "a voltage feedback path". However Kakuta discloses in Fig. 1 an analogous circuit having the claimed voltage feedback path. It would have been *prima facie* obvious to one of ordinary skill in the art at the time the invention was made to incorporate the teaching of Kakuta into the circuit of Behzad by having the claimed voltage feedback path. The ordinary artisan would have been motivated to modify the circuit of Behzad in the manner set forth for at least the purpose of achieving desired gain as mentioned by Kakuta in col. 1, lines 29-33, **meeting claim 5**.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Hieu Nguyen whose telephone number is 571-272-8577. The examiner can normally be reached on M-F 8-5.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert Pascal can be reached on 571-272-1769. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Hieu Nguyen
AU: 2817

hn

Robert Pascal
Primary Examiner